AMENDMENTS TO THE SPECIFICATION

1. Please replace paragraph [0013] with the following amended paragraph:

[0013] Please refer to Figs.4-9, which are schematic diagrams of fabricating contact holes on a semiconductor chip 50 according to the present invention. As shown in Fig.1, the semiconductor chip 50 has a substrate 52 comprising an array area 54 and a periphery area 56. The array area 54 is used for locating memory cells of a DRAM, and the periphery area 56 is used for locating the periphery controlling circuits of the DRAM. The semiconductor chip 50 also has an oxide layer 57~~(not shown)~~, a conductive layer 58, a silicide layer 60, and a first mask layer 62 on the substrate 52, wherein the oxide layer 57, composed of silicon dioxide (SiO2), serves as a gate oxide layer or a pad oxide layer of the ion implantation processes. The conductive layer 58 is composed of doped polysilicon. The first mask layer 62 can be formed by silicon nitride (SiN), silicon carbon (SiC), or silicon oxynitride (SiON). The forming method of the oxide layer 57, the conductive layer 58, the silicide layer 60, and the first mask layer 62 is well known to those skilled in the art, therefore no detailed description will be provided herein.

2. Please replace paragraph [0014] with the following amended paragraph:

[0014] As shown in Fig.5, before fabricating the

contact holes, the gates of the memory cells and periphery controlling circuits have to be fabricated in the array area 54 and the periphery area 56 respectively. At first, a PEP is performed to remove a portion of the first mask layer 62, the silicide layer 60, and the conductive layer 58 to form two gates 64, 66 in the array area 54 and a gate 68 in the periphery area 56. After that, a silicon nitride layer is deposited, and is then etchbacked through an anisotropic etching process to form a spacer 70 on the sidewall of each of the gates 64, 66, 68. An ion implantation and a thermal annealing process are performed to form a source and a drain 71~~(not shown)~~ of each of the gates 64, 66, 68.

3. Please replace paragraph [0017] with the following amended paragraph:

[0017] As shown in Fig.8, a glue layer 81~~(not shown)~~ is deposited and a metal layer 82, such as tungsten, is filled into the bit line contact hole 78 and the substrate contact hole 80. After that, a chemical mechanical polishing process or an etching process is performed to remove the metal layer 72 and the glue layer 81 above the second mask layer 74. As those skilled in the art may understand, the glue layer 81 is used for enhancing the adhesion force of the metal layer 82, and is composed of a titanium nitride (TiN) layer and a titanium (Ti) layer. Then, the second mask layer 74 is taken as a hard mask or an etching pad, and an etching process is performed for etching the first mask layer 62 through the gate opening 76 to

thereby form a contact hole 84. It should be noted that the first mask layer 62 and the second mask layer 74 are both removed by this etching process if the first mask layer 62 and the second mask layer 74 are composed of the same material. However, the main objective of this etching process is to remove the first mask layer 62 of the gate 68 not covered by the second mask layer 74. As a result, when the second mask layer 74 is thicker than or equal to the first mask layer 62, the main objective can be matched. That means although the second mask layer 74 may also be removed through this etching process, the first mask layer 62 on the top of the gates 64, 66 will not be damaged. According to another embodiment of the present invention, the first mask layer 62 and the second mask layer 74 are formed of different materials, and therefore an etching selectivity can be adjusted to only remove the first mask layer 62 not covered by the second mask layer 74 and leave the second mask layer 74 whole. Thus, the thickness of the second mask layer 74 does not have to be greater than that of the first mask layer 62.